



SSC8125GS6

P-Channel Enhancement Mode MOSFET with ESD Protection

➤ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$ Typ.	I_D	ESD
-20V	$\pm 8V$	36mR @-4.5V	-4A	3kV
		45mR @-2.5V		
		57mR@-1.8V		

➤ Description

This device uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.5V and it is protected from ESD. These features make it suitable for use as a load switch or in PWM applications.

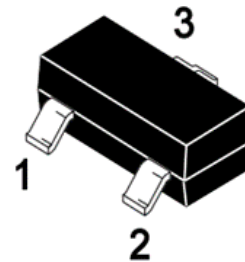
➤ Applications

- Load Switch
- Portable Devices
- DCDC Conversion

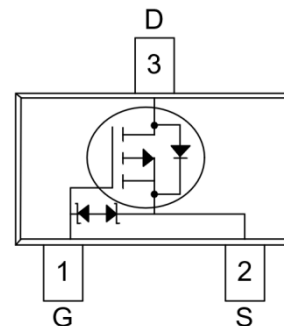
➤ Ordering Information

Device	Package	Shipping
SSC8125GS6	SOT-23	3000/Reel

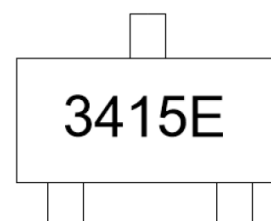
➤ Pin configuration



SOT-23



Pin Configuration (Top View)



Marking



➤ **Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-20	V
V_{GSS}	Gate-to-Source Voltage	± 8	V
I_D	Continuous Drain Current ^a	-4	A
I_{DM}	Pulsed Drain Current ^b	-20	A
P_D	Power Dissipation ^c	0.9	W
P_{DSM}	Power Dissipation ^a	0.45	W
T_J	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance		280	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		140	

Note:

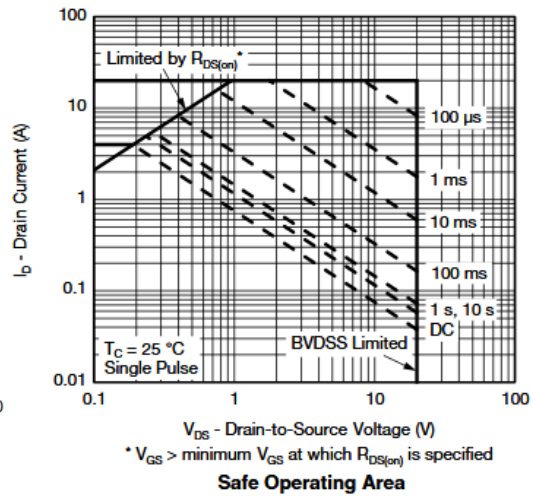
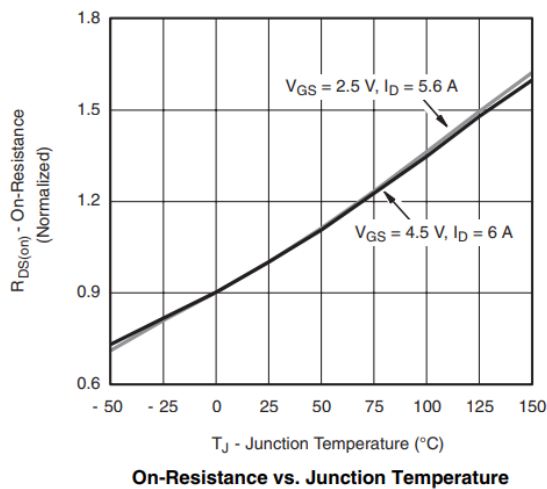
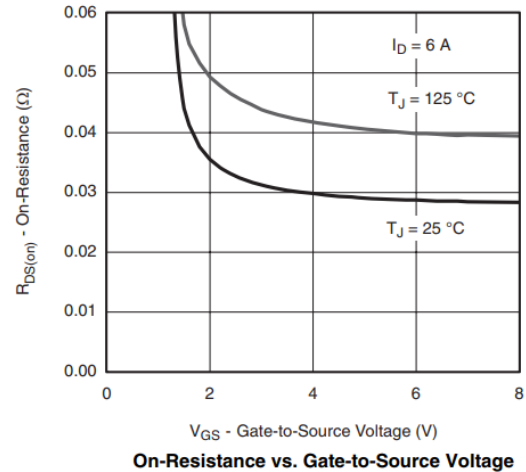
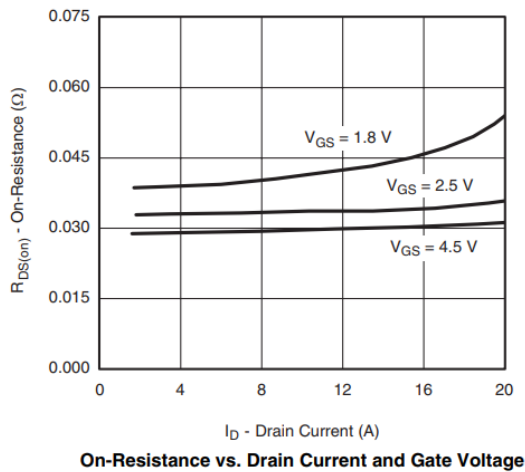
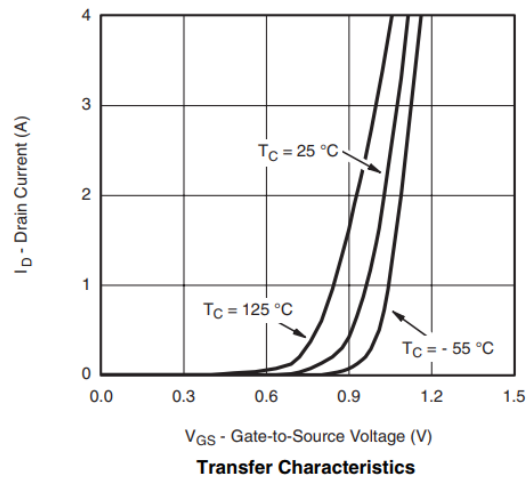
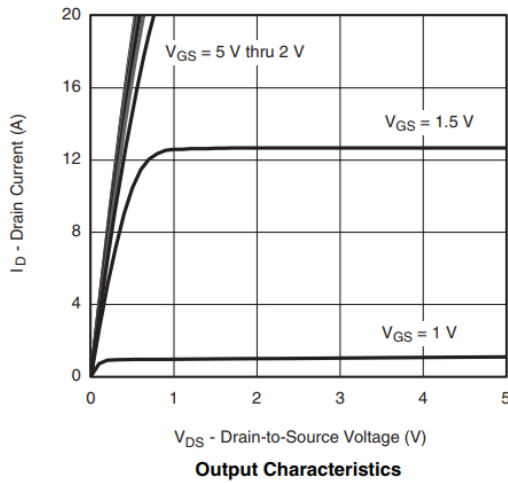
- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user is specific board design. The power dissipation is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

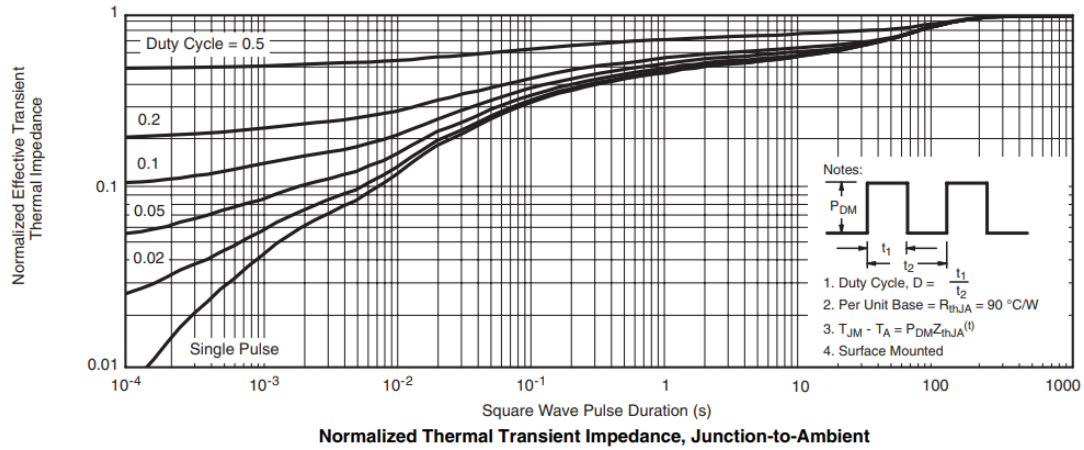
**➤ Electrical Characteristics (T_A=25°C unless otherwise noted)**

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.4	-0.6	-1	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-4A		36	41	mΩ
		V _{GS} =-2.5V, I _D =-3A		45	52	
		V _{GS} =-1.8V, I _D =-2A		57	62	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			-1	μA
Gate-Source Leak Current	I _{GSS}	V _{GS} =±8V, V _{DS} =0V			±10	uA
Forward Voltage	V _{SD}	V _{GS} =0V, I _S =-1.6A		-0.7	-1.3	V
Input Capacitance	C _{ISS}	V _{DS} = -10V, V _{GS} = 0V, f = 1MHz		418		pF
Output Capacitance	C _{OSS}			136		
Reverse Transfer Capacitance	C _{RSS}			56		
Turn-on Delay Time	T _{D(ON)}	V _{GS} =-5V, V _{DS} =-10V, RL=1.5R, RG=3R		18		ns
Rise Time	T _r			12		
Turn-off Delay Time	T _{D(OFF)}			70		
Fall Time	T _f			25		

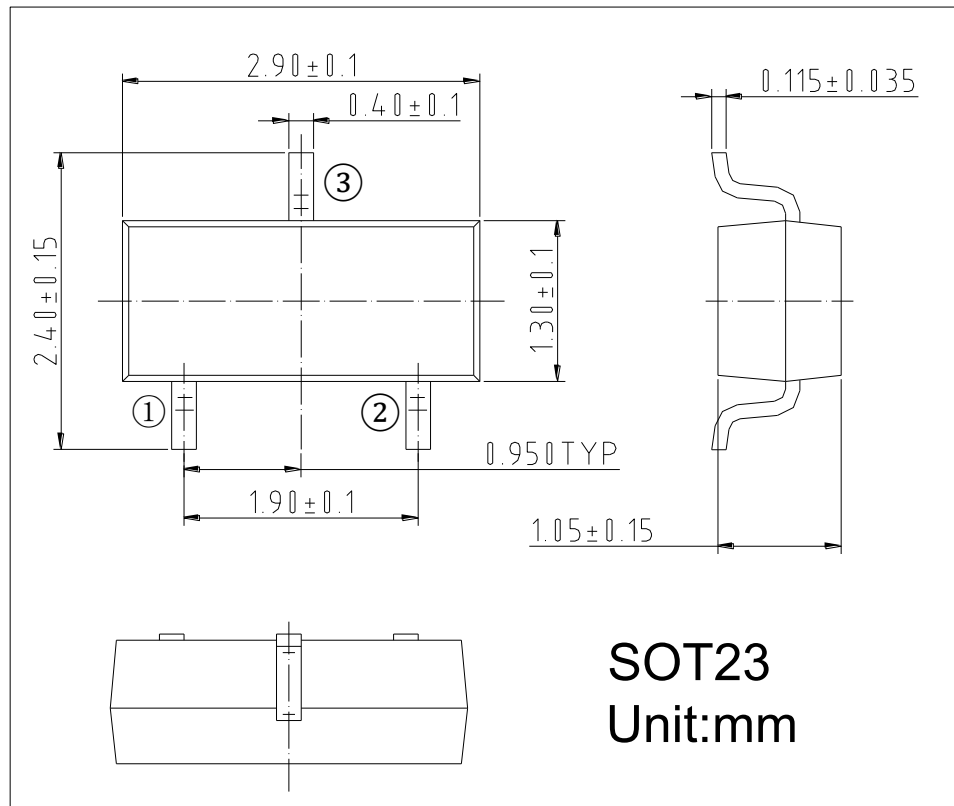


➤ Typical Performance Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)





➤ Package Information



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